HIGH EFFICIENCY FLYBACK CONVERTER

Cross Reference to Related Applications

Priority is claimed from U.S. provisional patent application Serial No. 60/372,280 entitled "High Efficiency Flyback Converter" filed April 12, 2002 in the name Ionel D. Jitaru. That application is incorporated herein by reference.

Field of the Invention

This invention relates to DC-DC flyback converters and more particularly to a DC-DC flyback converter having a controlled synchronous rectifier in a secondary circuit and the means of controlling the synchronous rectifier.

Background of the Invention

Of available DC-DC converters used for power conversion purposes, the flyback converter is the most simple. Its minimum configuration consists of only a switch, a transformer, a diode and two capacitors (one at the input port and the second one at the output port). In low-output-voltage converters, the conduction loss of the diode rectifier due to its forward voltage drop becomes the dominant power loss. In certain conditions this loss can reach 50% of the total power loss. The simple approach conceived to reduce the above-mentioned power loss was to replace the rectifying diode with a synchronous rectifier, i.e. with a low-ON-resistance MOSFET. To perform the normal operation of the flyback converter the control of the MOSFET used as the synchronous rectifier is easily obtained by inverting the primary main switch control signal. Fig. 1 shows such an approach. There an input voltage source 2 supplies a series-connected primary winding 6 of a transformer 4 and a primary switch S1. A control signal Vc(S1) for the switch S1 is constant frequency control signal having a variable ON duty-cycle to assure a stable output voltage. To the output circuit, a secondary winding 8 of the transformer 4 provides a voltage 10 that alternates in polarity. The synchronous rectifier S2 couples an output load circuit comprising a load 24 and a filtering capacitor 22 to the output voltage 10 during the OFF time of S1's switching period. A synchronous rectifier S2 receives a control signal Vc(S2) through an inverter 26.

Because of its effect during operation of the circuit, the body diode 18 of the MOSFET that is used as a synchronous rectifier is also shown in Fig. 1.

Fig. 1A displays the voltages and currents versus time waveforms for the flyback circuit parameters, i.e., Vc(S1), the control signal for the switch S1; Vc(S2), the control signal for switch S2 or synchronous rectifier; I(S1), the current through the switch S1; I(S2), the current through the switch S2 and V(S2), the voltage across the switch S2, for continuous-conduction mode (CCM). Fig. 1B displays the voltages and currents versus time waveforms for the discontinuous-conduction mode of operation (DCM). Fig. 1C depicts the same waveforms for the critical conduction mode of operation, the limit case between continuous mode and discontinuous mode of operation.

The main drawback of the above presented approach is the cross-conduction (concurrent conduction) of the primary switch S1 and secondary synchronous rectifier S2 for the time intervals t_0-t_1, t_2-t_3 (see Fig. 1A), for CCM operation. As a result, during these time intervals when the body-diode 18, an intrinsic part of the synchronous rectifier S2, is ON, supplementary power losses appear and have to be taken into account. Another drawback is related to power loss introduced by the reverse recovery, during t_3-t_4, of the body-diode 18 during turn-off of the primary switch S1, which adds to the general power balance or total power use of the circuit.

For DCM operation, See Fig. 1B, the power loss due to reverse recovery process of the body-diode 18 is eliminated because the current of the synchronous rectifier S2 becomes zero before the primary switch S1 is turned "on," but the cross-conduction process during turn-off of switch S1 still exists. There are two drawbacks related with this mode of operation: higher conduction loss during Td (ON), see Fig. 1C, due to cross-conduction of I(S1) and I(S2) and the fact that the circuit efficiency fluctuates with Vin of the input voltage source 2.

The critical conduction mode of operation offers in certain conditions a zero voltage switching or ZVS feature which can be used if a proper design of the circuit is made. In this case the recover loss is eliminated also but the higher conduction loss associated with cross-conduction of I(S1) and I(S2), during Td(ON) delay, is still important.

There is a need therefore for a DC-DC flyback converter having a synchronous rectifier in its secondary circuit that is controlled such that cross-conduction losses are eliminated or substantially eliminated and reverse recovery losses are eliminated or substantially eliminated.

Summary of the Invention

In order to address the drawbacks of the prior art, the present invention provides an improved driving circuit that reduces power loss due to cross-conduction process.

In accordance with a preferred embodiment of the present invention, a driving technique is provided which improves the efficiency of a flyback DC-DC converter using a synchronous rectifier in the output section or secondary circuit by processing in a certain sequence information related to the primary switch control, the voltage across the secondary winding of the power transformer and the voltage across the synchronous rectifier to obtain a final control signal for the synchronous rectifier.

In one embodiment of the present invention, the control circuit for a synchronous rectifier in the secondary circuit comprises a logic circuit that uses the control signal that is used to control the main switch or primary switch in the primary circuit and the voltage derived from a secondary winding of a main transformer coupling the primary and secondary circuits. The logic circuit also uses the voltage across the synchronous rectifier to form a third input to the logic circuit. The signals developed turn ON and turn OFF the synchronous rectifier. More specifically, the logic circuit of the embodiment of the invention just described includes an AND gate to which a voltage derived (inverted)from the main switch control signal is applied along with outputs from first and second bistable circuits. The first bistable circuit is supplied an input from a first comparator to which the voltage derived from a main transformer secondary winding is applied. The second bistable circuit has an input from a second comparator to which is supplied the voltage across the synchronous rectifier. To the first and second bistable circuits the main switch control voltage is applied as a second input. In this way the main switch control signal turns OFF the synchronous rectifier and the voltage across the secondary winding turns ON the synchronous rectifier. Reference inputs to the comparators typically are set at substantially zero volts. In the

preferred embodiment that uses the logic circuit to develop the synchronous rectifier control, typically the first and second bistable circuits, are first and second RS flip-flops. The voltage derived from the first control signal is applied to the "set" or S input of each of the flip-flops. To the "reset" or R inputs are applied the outputs of the first and second comparators, respectively. The first flip-flop has its "set" or Q output applied as an input to the AND gate and the second flip-flop has its "reset" or Q output applied as an input to the AND gate.

The method of controlling induction of the synchronous rectifier in the secondary circuit of a DC-DC flyback converter, then, preferably includes turning on the synchronous rectifier in dependence on establishment of a voltage across a transformer secondary winding of the main transformer that couples the secondary circuit to the primary circuit and turning OFF the synchronous rectifier in dependence on turning ON the main switch in the primary circuit. Turning OFF the synchronous rectifier in dependence or the turning ON of the main switch preferably comprises turning OFF the synchronous rectifier when the main switch is turned "on." As previously described the method can include providing a logic circuit connected with the control electrode of the synchronous rectifier for the application of the voltage derived from a voltage across a secondary winding as one input to the logic circuit and applying a voltage derived from a main switch control signal as a further input to the logic circuit. In a preferred embodiment the third input to the logic circuit is a voltage derived from a voltage across the synchronous rectifier.

The method of a specific, exemplary preferred embodiment can be utilization of the logic circuit as described in greater detail above in connection with the use of an AND gate, a pair of bistable circuits, and supplying the main switch control signal to an inverter connected with the AND gate. In this method, the provision of the bistable circuits can be the provision of first and second RS flip-flops as previously described. Also as previously described the method can include the application of the specific inputs to the set and reset inputs of the flip-flops and the specific set and reset outputs applied to the AND gate.

In a further embodiment of the invention the secondary winding from which the control signal for the synchronous rectifier is in part derived can be a control secondary winding wound on a magnetic core that serves as the main transformer core, the

magnetic core having a center flux path dividing into two outer flux paths onto which the secondary winding is wound in current canceling relation as to flux that is conducted from the center flux path to the two outer flux paths. A primary control winding on at least one of the two outer flux paths is supplied an input derived from the main switch control voltage.

In a preferred embodiment the main switch control voltage is differentiated and the differentiated signal is applied to the control primary winding input. In this preferred embodiment, the main switch control signal is substantially a square wave.

In one specific exemplary preferred embodiment, the control voltage developed in the control secondary winding of the embodiment of the invention just described is applied to a switching circuit connected in controlling relation to the synchronous rectifier. The switching circuit may be a transistor switching circuit. In the case of a transistor switching circuit, a DC bias voltage can be developed from a secondary winding of the main transformer and applied to the transistor switching circuit for the purpose of applying a DC bias thereto. In each of the preferred exemplary embodiments described, the synchronous rectifier can be a MOSFET switch. Where a transistor switching circuit is connected to control the synchronous rectifier, it can be connected to the gate of the MOSFET switch. One preferred embodiment of a suitable transistor switching circuit is a serially connected PNP and NPN transistor pair connected between the DC bias voltage and ground, the junction of the transistor pair being connected to the gate of the MOSFET switch.

A preferred embodiment of a DC-DC flyback converter in accordance with the invention is a flyback converter having, as previously described, a synchronous rectifier in its output or secondary circuit to which is supplied a control signal derived from a voltage across a control secondary winding that is wound upon two outer flux paths of a magnetic core serving as the magnetic core of the main transformer and arranged such that flux conducted from a center flux path into the outer flux paths develops substantially no current in the control secondary winding. A control primary winding is wound onto at least one of the two outer flux paths and preferably, in one preferred embodiment, onto each of the two outer flux paths in current canceling relation with respect to the flux conducted to the outer flux path from the center flux path. An input to a circuit supplying the control primary winding with an input taken from the primary

or main switch control signal is, preferably, a differentiation circuit connected between the control of the main switch and the control primary winding. In this flyback converter, the control signal applied to the synchronous rectifier can be supplied by the switching circuit described above. Again, the switching circuit can be a transistor switching circuit and can have a bias potential applied thereto taken from a DC bias circuit connected with a secondary winding and including at least one rectifying diode. The turning ON and OFF of the transistors that make up the transistor switching circuit is, of course, taken from the control secondary winding.

In the preferred exemplary embodiments described herein, power losses due to cross conduction between the main switch and the synchronous rectifier can be eliminated or nearly entirely eliminated and reverse recovery losses can likewise be eliminated or nearly entirely eliminated.

Both of the above-described embodiments of the present can be implemented by using either a separate transformer or one integrated with the main transformer. The transformer can be discrete component of its own or can be imbedded in a PCB carrying the converter circuitry. The driving transformer in both embodiments can be embedded into the main transformer of the converter.

The foregoing and other objects, features and advantages of the present invention will be more readily understood upon consideration of the following detailed description of the invention together with the following drawings.

Brief Description of the Drawings

Fig. 1A is a schematic of a prior art flyback converter with a synchronous rectifier in the output section;

Fig. 1B is a series of plots of the main voltage and current waveforms, versus time, for the continuous-conduction mode of operation or CCM of the prior art converter of Fig. 1A;

Fig. 1C is a series of plots of the main voltage and current waveforms, versus time, for the discontinuous-conduction mode of operation or DCM of the prior art converter of Fig. 1;

Fig. 1D is a series of plots of the main voltage and current waveforms, versus time, for the critical-conduction mode of operation, the limit case between CCM and DCM, of the prior art converter of Fig. 1;

Fig. 2 illustrates the basic schematic of the flyback converter with synchronous rectifier in the output section according to this invention;

Fig. 3 is a schematic of a synchronous rectifier like that of the converter of Fig. 2 including the control according to this invention;

Fig. 4A is a series of plots of the main voltage and current waveforms, versus time, for the continuous-conduction mode of operation or CCM of the converter of Fig. 2 according to this invention;

Fig. 4B is a series of plots of the main voltage and current waveforms, versus time, for the discontinuous-conduction mode of operation or DCM of the converter of Fig. 2 according to this invention; and

Fig. 5 is a series of plots of the driving technique of the synchronous rectifier of the converter of Fig. 2 according to this invention.

Detailed Description

The approach used to control the synchronous rectifier of a DC-DC flyback converter according to this invention is first described in relation to the improved basic schematic of the flyback converter shown in Fig. 2. In the flyback converters of Figs. 1 and 2, like elements bear like reference numerals. The voltage source 2 supplies the input circuit formed by the primary winding 6 of the power transformer 4 connected in series with the switching MOSFET S1. The switching transistor S1 is controlled by a signal Vc(S1). The output circuit of the flyback converter contains the secondary winding 8 of the power transformer 4 connected in series with the synchronous rectifier S2 and the output load 24. The output voltage obtained on the load is filtered by the capacitor 22. The body diode 18 of the synchronous rectifier is also represented as it plays a role in the operation of the circuit. According to one preferred embodiment of this invention, besides the main switch control signal Vc(S1), which controls the main input switching transistor S2 in Fig. 1, two supplementary signals are used to process the final controlling signal Vc(S2) for the output synchronous rectifier S2. These are

the voltage 50, Vs(+)-Vs(-), across the secondary winding and the voltage Va-b across the synchronous rectifier S2. This is described with reference to Fig. 3.

In Fig. 3 a control section 100 is used to process digitally the signal Vc(s2). The main switch control signal Vc(S1) is first coupled through an inverter 101 to the multiple input AND gate 116. Also the signal Vc(S1) is coupled to the "set" (S) inputs of two bistable circuits 112 and 114. These may be RS flip-flops as shown. The voltage 50 across the secondary winding 8, Vs(+)-Vs(-), is coupled to the non-inverting input (+) of a comparator circuit 102. On the inverting input (-) is coupled a reference signal Vref1, which typically is equal to zero, but could have a non-zero value also. The output signal of the comparator circuit 106 is connected to the "reset" (R) input of the bistable circuit 114. The output "set" (Q) state of the bistable circuit 112 and the output "reset" ($\overline{Q}$) state of the bistable 114 are each connected to one of the multiple inputs of the AND gate 116. The output of the AND gate 116 provides the control signal Vc(S2) for the synchronous rectifier S2. The main features this circuit assures are: the turn ON of the synchronous rectifier S2 is provided by the voltage 50 on the secondary winding, Vs(+)-Vs(-), and turn OFF is by the information coming from the primary side, Vc(S1). Cross-conduction of the main switch S2 and the synchronous rectifier S2 is avoided.

Fig 4A depicts the main voltage and current waveforms versus time for the converter of Fig. 2 operating in continuous-conduction mode and with the improved control of the digital logic circuit depicted in Fig. 3. Fig. 4A shows the drain-source voltage Vds(S1) on the main primary switch S1. Also shown is the voltage on the secondary winding Vsec (Vs(+)-Vs(-)), which takes into account the delay produced in the transformer by the leakage inductance and the level of the current through it. Fig. 4A shows, as well, the effect on the control signal Vc(S2) produced by a heavy or a light load. I(S2), the current through the synchronous rectifier is also shown in Fig. 4A. Shown in broken lines is the reverse current 30 eliminated by the "adjustable" turn ON by Vc(S2) of the synchronous rectifier to eliminate reverse recovery losses.

Fig. 4B depicts the main voltage and current waveforms versus time for the converter of Fig. 2 operating in discontinuous-conduction mode, and with the improved control of the digital logic circuit depicted in Fig. 3. Fig. 4B shows the drain-source voltage Vds(S1) on the main primary switch S1. Also shown is the voltage on the

secondary winding, Vsec (Vs(+)-Vs(-)), which again takes into account the delay produced in the transformer by the leakage inductance and the level of the current through it. Fig. 4B shows, as well, the voltage Vds(S2) across the synchronous rectifier S2 and the effect on the control signal Vc(S2) produced by a reduced load.

Another embodiment of this invention is exemplified by the driving technique used to control the synchronous rectifier S2 as depicted in Fig. 5. The driving technique can make use of a transformer separate from the main transformer, or transformer windings integrated with the main transformer as illustrated in Fig. 1. Either way, the transformer can be a discrete transformer or a planar transformer imbedded in a PCB. An input signal source 60 is applied through a derivative or differentiation (dv/dt) RC circuit 62, 64 to a control primary winding 66 wound on the outer flux paths 70, 74 of an E+I magnetic core assembly 76, 80. The input signal 60 is ordinarily the control signal for the main switch S1 connected in the input, primary circuit (as shown in Fig. 1). Fig. 5A plots, at 61, the voltage of source 60 at point A in Fig. 5, and its derivative, at 63, provided at point B in Fig. 5 vs. time. The main windings 78 of the power transformer are wound on the center leg 72. Control secondary winding 68 is also wound on the outer flux paths 70, 74. The control secondary winding 68 is wound on the outer flux paths such that flux passing into the outer flux paths from the center flux path of the leg 72 results in substantially no current in the winding 68. In the embodiment of Fig. 5, the control primary winding 66 is similarly wound. Flux produced in the outer flux paths 70, 74 cancel in the center leg 72. In this way the windings 66, 68 of the driving transformer produce a magnetic field that doesn't interfere with the main one produced by the power transformer as long as the driving field is not too high, and the control secondary winding current is the result of substantially only the control primary winding excitation. The output signal produced by the secondary winding 68 is applied to a totem-pole structure made by serially connected NPN transistor 84 and PNP transistor 82, which structure delivers the control signal to the synchronous rectifier 86. The totem-pole structure is supplied with a biasing DC voltage produced by an auxiliary winding 90. This is preferably also wound on the main transformer and is rectified with a rectifying diode 88. The operating characteristics of this embodiment are essentially the same as those of the converter operated under control of the circuit of Fig. 3, as plotted in Figs. 4A and 4B.

A main advantage of this embodiment as shown is the simplicity of the driving circuit. At the same time the integrated option offers the lower cost which can be obtained because the synchronous rectifier 66 and 68 driving windings are designed and made together with main windings 78 of the power transformer. Note that the "outer flux paths" on which the windings 66 and 68 are wound include not just the outer legs 70 and 74 but the entire magnetic structure forming the two paths out of and then returning to the center leg. In other words either or both windings 66 and 68 can be wound on the upper or lower paths adjoining the center leg as shown in Fig. 5 as well as on the two outermost legs of the magnetic core 76, 80.

The foregoing descriptions of preferred embodiments are exemplary and not intended to limit the invention claimed. Obvious modifications that do not depart from the spirit and scope of the invention as claimed will be apparent to those skilled in the art. For example, although the logic circuit of Fig. 3 uses specific bistable circuits and gate, other logic element may be arranged to accomplish the same or a similar output from the inputs applied. And in the embodiment of Fig. 5 "E" and "I" magnetic core elements are employed, but a toroid bridged by a central leg could provide the outer flux paths and the center leg for example. Switching circuits other than the series connected transistors 82 and 84 may be effectively employed as well.